EMLC 2024 - the "European Mask and Lithography Conference" held in Grenoble

This year's EMLC took place (now for the 4th time) from 17 - 19 June in the beautiful and modern conference centre of the MINATEC Campus (Micro and Nanotechnology Innovation Center) in Grenoble (France). The approximately 170 participants from all over the world were offered a broad and densely packed programme with 72 presentations. These were divided into 4 keynotes, 44 lectures - 17 of which were invited and 8 student presentations - 2 tutorials and 22 posters, 8 of which were student presentations (which corresponded to the content of the lectures). This is once again significantly more than last year and is a sign of the growing relevance of (and interest in) this conference.

As always, the keynotes provided an overview of the development directions and trends in the semiconductor industry and the related fields of micro and nano technology. While last year's focus was on limiting the excessive energy consumption of current and future AI applications, the keynote by Serge Nicoleau (ST Microelectronics) extended this topic to the general sustainability of processes in the semiconductor industry, i.e. reducing resource consumption and increasingly avoiding toxic or environmentally harmful substances such as PFAS (so-called eternal chemicals). Further keynotes by Kagawa-san (Canon), Sebastian Dauvé (CEA-LETI) and Kurt Ronse (IMEC) dealt with the current status and outlook for nano-imprint lithography, the semiconductor research programme at CEA-LETI (FAMES) and EUV lithography. Kurt Ronse's contribution in particular provided a preview of the expected development in nanotechnology up to the year 2040. While leading companies in the semiconductor industry are about to introduce high-end processes with the technology node N2 (where, for example, the conductor tracks in the densest wiring levels have a width of around 11nm), a line width of only around 6nm (!) will be achieved in node A1 (according to the current roadmap in 2040).

In the other 8 lecture sessions and the poster session, the conference focussed in detail on current problems and advances in DUV (deep ultraviolet) and EUV (extreme ultraviolet) lithography, NIL (nanoimprint lithography), mask production, metrology and inspection as well as other applications of lithographic technologies such as the production of photonic circuits or components for quantum computers. We don’t go into the basics of these technologies here, but they are easy to find on Wikipedia, for example.

The central topic of several presentations were reports on the status of High-NA EUV development. As in all optical technologies, the resolution of EUV (corresponding to the Abbe resolution limit) depends on the wavelength used - 13.5 nm for EUV - and the numerical aperture of the optical system - NA=0.33 for the current generation of devices. If better resolution is to be achieved at the same wavelength, the numerical aperture must be increased, to 0.55 for the next generation of devices. Despite the extreme challenges that had to be overcome for the realisation of high-NA exposure devices (details can be found in the conference reports of previous years), the contributions from ASML and IMEC now show that the first High-NA devices are operational and deliver the expected results.

In a further presentation by Jan Van Schoot (ASML), the entire spectrum of tasks to be solved again and again was made clear in one sentence: "Key to continue Moore's law: Resist, Dose, Contrast". The aforementioned numerical aperture (NA) is an important (but not the only) parameter for achieving sufficient contrast when imaging ever smaller structures. It is therefore not surprising that the next step towards increasing the NA is now being considered and reported on; a value of NA=0.75, called Hyper-NA, is being discussed. The currently available EUV sources provide enough power for a high throughput of the current devices, but at an already high price: approx. 1.5 MW of electrical power must be

used for the approx. 1000W EUV power. For various reasons, a hypothetical hyper-NA device would require significantly more power. This is where a particularly exotic idea comes into play: EUV light is currently generated using a plasma source (drops of liquid tin are heated by a sequence of laser pulses to such an extent that a plasma is created, which then emits the EUV radiation). However, radiation of the same wavelength can also be generated using a suitably dimensioned free electron laser (FEL). As this primarily requires an electron accelerator, the "suitable dimensions" are in the order of a few 100 meters. For the same EUV power of 1000W, however, only an electrical power of approx. 200kW would have to be used; further advantages would be found in specific optical properties such as polarization. The future will show where the journey will take us.

Another approach to achieving a sufficiently good contrast is a technology known as "inverse lithography". With the help of an exact model of the imaging system, a reverse calculation is made of what the geometry on a mask must look like in order to create the desired image on the silicon wafer. The geometry of a circuit is usually represented as "Manhattan geometry" - i.e. consisting of rectangles and lines parallel to the axes or slanted to 45°. Inverse lithography results in "ideal" structures on the mask having curvilinear edges and only a distant similarity to the geometry that is to be created on the wafer. This has considerable consequences for the writing of such structures on the mask and for the measurement of such structures for quality assessment (see metrology below). In order to be able to efficiently describe such structures, which no longer have straight edges, a new standard for a suitable data format had to be developed, which has now been given the name SEMI P49 (OASIS with multigon extension). Initial experiences with this standard and further progress in this area were presented, particularly in contributions from Siemens Digital Industries Software, IMEC, Intel and IMS Nanofabrication. The next step will probably be to use curvilinear descriptions in the design systems from the beginning and - at least for high-end chips - to move away completely from the Manhattan geometry that has dominated up to now. The electron multibeam mask writers from IMS Nanofabrication and Nuflare, now in their third generation, with their ability to generate these structures now and in the future in a tolerable writing time and with the necessary accuracy, were presented in separate contributions.

The generation of the structures on the mask and their imaging on wafers is closely related to the corresponding measurement technology - metrology - which is used to verify for each mask that the structures written on the mask are the right size and in the right places - both light-optical and electron microscopes (CD-SEM) are used for this purpose. Line widths (CD - Critical Dimension), position and many other parameters are measured. The current challenge is that the structures to be measured are no longer lines and rectangles, so what can be measured at all? A whole series of papers and posters from Zeiss, Advantest, IMEC and others presented approaches and solutions that use significantly more CD-SEM measurements and new evaluation algorithms to describe the dimensional accuracy of structures with an EPE (Edge Placement Error) value, regardless of how straight or curved the measured edges really are. Incidentally, this is also an important field of application for machine learning and AI programs, as was shown in several contributions to the Data Analytics Session, which also dealt with AI-supported fab control and process models.

Several contributions highlighted the efforts that need to be made to provide resists that can keep pace with the ever-improving resolution of lithography devices. For some years now, research has been carried out on resists whose complex molecules have metal-oxide components embedded in them, which favors good absorption and small molecule sizes - necessary prerequisites for being able to render the resolution possible with High-NA scanners in the resist. A remarkable student presentation from Fraunhofer IISB (Erlangen)

was dedicated to the simulation of so-called multi-trigger resist materials, which are gaining increasing interest, also for High-NA EUV lithography.

In the sessions and contributions at this conference, it was also clear that although the biggest (and foreseeably most expensive) innovations are taking place in the High-NA-EUV and related areas, the largest quantities of masks, semiconductors and other products in the nano industry are being manufactured using so-called "mature technologies" - and here, too, constant progress is being reported.

For KrF and ArF scanners (248nm and 193nm respectively), for example, new peak values for throughput and overlay are being achieved with advanced imaging optics, illumination systems and other innovations.

A whole range of applications, particularly in the manufacture of photonic and nano-optical components, can benefit from performance improvements in Vistec VSB (Variable Shaped Beam) electron beam pattern gererators as shown in contributions from IMS- CHIPS (Stuttgart) and Fraunhofer IOF (Jena).

This year's "Zeiss Award for Talents in Photomask Industry", which is awarded to the best student contribution, went to Nicolas Triomphe et al. (Univ. Grenoble Alpes / CEA-LETI) for his paper "Self-assembly of shape-complementary DNA origamis for lithography applications". The EMLC 2024 Best Paper Award went to Lieve Van Look et al. (IMEC) for her paper "Stitching at resolution for High-NA: an experimental process window study", while the EMLC 2024 Best Poster Award winner was Matthias Roesch et al. (Carl Zeiss SMT GmbH) with "Quantitative access to phase-effects in High-NA photomasks using AIMS® ".

The 40th edition of the EMLC conference will take place in Dresden in June 2025.

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